

End-to-End Quantization Co-Design for MHz GaN Converters using Dither and Sigma-Delta Modulation

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Abstract: We study end-to-end quantization in digitally controlled MHz-range GaN DC–DC converters, spanning the analog-to-digital converter (ADC), fixed-point controller, and digital pulse-width modulator (DPWM). A simulation framework sweeps ADC and DPWM resolutions across buck, boost, and inverting buck–boost converters at 1, 5, and 10 MHz, reporting regulation bias, output ripple, and limit-cycle occurrence. A simple metric ρ compares the DPWM step (mapped to V_{out}) to the ADC least-significant bit and accurately predicts the onset of limit cycles: designs with $\rho \geq 1$ avoid limit cycles in all surveyed cases. The results yield practical rules: boost and buck–boost require finer DPWM than buck due to larger $\partial V/\partial D$; dithering and first-order sigma–delta ($\Sigma\Delta$) modulation provide roughly one to two effective DPWM bits at 1 MHz; and increasing switching frequency tightens timing margins but can be offset by modest DPWM resolution or reduced digital delay. Validation includes analytic–simulated slope agreement, ρ –versus–limit-cycle slices, and robustness to parasitic spreads, ADC noise, and jitter. These findings provide concise, quantitative guidance for selecting ADC and DPWM resolutions to meet ≤ 10 – 20 mV ripple targets without limit cycles in MHz GaN converters.

Keywords: GaN, DC–DC converters, digital control, quantization, Limit Cycles, DPWM

1. Introduction

GaN switches make MHz switching practical and unlock impressive power density and transient speed in DC–DC converters. The price, however, is a far tighter digital control problem. In a fully digital loop, the analog-to-digital converter (ADC) samples the output into discrete codes, a fixed-point controller updates the duty command, and a digital pulse-width modulator (DPWM) turns that command into on/off pulses. Each block introduces quantization that behaves like a nonlinear disturbance. Classic analyses show that these quantizers can drive limit-cycle oscillations (LCOs) with poorly predictable frequency and amplitude [1], complicating electromagnetic interference (EMI) behaviour. At the same time, tight regulation targets on the order of a few millivolts demand high ADC and DPWM resolution [2], which costs power and area.

This work focuses on end-to-end co-design of resolution across the ADC, controller arithmetic, and DPWM for converters operating in the MHz range. We revisit how coarse quantization affects steady-state accuracy, dynamic response, stability margins, and EMI, and we ground the discussion with simulation evidence and simple design rules that generalize across topologies. Our discussion builds on prior studies of quantization-induced LCOs and resolution trade-offs [3] and [4], but emphasizes practical guidance for modern GaN converters.

1.2 Literature Survey

Digital control of switch-mode converters has a deep literature showing how finite DPWM and ADC resolution

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Table 1. Representative studies on quantization in digitally controlled DC–DC converters.

Reference	Topology	f_{sw}	ADC (bits)	DPWM (bits)	Key findings
Prodić et al., 2001 [5]	Buck	1 MHz	8–10	8–10	Early digital buck implementation and practical guidance on ADC/PWM resolution to meet output accuracy.
Patella et al., 2003 [2]	Buck	1 MHz	6	6 (+ dither)	Demonstrated repeating duty patterns (dither) to realize ~12-bit effective resolution at 1 MHz.
Peterchev & Sanders, 2003 [1]	Buck (model)	–	Variable	Variable	Analyzed steady-state LCOs from ADC/DPWM quantizers; derived no-LCO conditions and introduced controlled DPWM dithering.
Peng et al., 2007 [3]	Buck (model)	–	Variable	Variable	Developed static and dynamic quantizer models; provided design criteria linking ADC/DPWM bits and loop gain for no-LCO behavior.
Lukić et al., 2007 [4]	Buck (IC)	>10 MHz	6	≥ 6 (multi-bit $\Sigma\Delta$)	Proposed a multi-bit $\Sigma\Delta$ PWM controller with fine effective duty resolution beyond 10 MHz and reduced low-frequency ripple via noise shaping.

Alters loop gain and can even induce limit cycles; these fundamentals and their design implications are well established in classic and modern references [1, 6–8]. Practical guidance on budgeting resolution, latency, and sampling—together with implementation tips for real power stages—appears in seminar and monograph treatments [9, 10], [11]. Recent studies quantify how ADC quantization propagates through cascaded current/voltage loops and affects accuracy and stability, while also surveying remedies for low-resolution limit cycling [12], [13]. On the implementation side, a wide range of DPWM architectures—from ASIC to FPGA with sub-clock interpolation—has been developed to push effective time resolution; these works review alternatives, identify trade-offs, and demonstrate concrete techniques for fine duty-cycle granularity [14], [15].

Timing jitter and switching uncertainty shift effective duty cycle, impact efficiency, and tighten timing budgets, motivating both analysis and mitigation in digital controllers [16]. To curb EMI while preserving regulation bandwidth, spread-spectrum and related frequency-modulation strategies have proven effective, with recent results clarifying co-existence and limits in practical systems [17], [18], [19]. Pushing into the multi-MHz regime—often with GaN devices—exposes new trade-offs among parasitics, sampling delays, and quantization; demonstrations span very-high-frequency prototypes and PWM-controlled MHz converters [20], [21]. Modern digitally controlled converters also illustrate mode-management features such as automatic PFM–PWM transition to protect light-load efficiency without sacrificing precision at higher loads, and scaling to interleaved, traction-class GaN systems highlights the approach’s practicality at power and phase count [22], [23].

Table (1) reviews representative studies on quantization in digitally controlled DC–DC converters. Early demonstrations by Prodić et al. showed 1 MHz digital buck operation with practical guidance on allocating ADC and PWM bits [5]. Patella et al. introduced repeating duty patterns (dither) to achieve near 12-bit effective resolution from a 6-bit base at 1 MHz [2]. Peterchev and Sanders analysed how ADC and DPWM quantizers drive

steady-state limit cycles (LCOs) and derived conditions to avoid them, including the use of controlled dithering [1]. Peng et al. extended the modelling to static and dynamic quantizers, linking no-LCO behaviour to the interplay among ADC/DPWM resolution and loop gain [3]. At higher frequencies, multi-bit $\Sigma\Delta$ PWM was proposed to improve effective duty resolution and shape low-frequency artefacts [4].

Overall, the literature establishes two themes: (i) adequate resolution or spectrum-shaping techniques (dither, $\Sigma\Delta$) can mitigate quantization limits, and (ii) quantization interacts with closed-loop dynamics in nonlinear ways that simple linear margins do not capture. The gap this work addresses is an end-to-end, cross-topology view that ties ADC resolution, fixed-point controller arithmetic, and DPWM realization together under MHz timing constraints, and distils the outcome into simple, testable design rules. In particular, we show that a single interpretable metric, ρ (the ratio of the ADC LSB to the DPWM step mapped through $\partial V/\partial D$), closely predicts the LCO boundary across buck, boost, and inverting buck-boost, and that dither/ $\Sigma\Delta$ recover roughly one to two effective DPWM bits at 1 MHz.

2. Modeling and Methods

This section describes the non-ideal plant model, the digital control chain (ADC, fixed-point controller, DPWM with dither and $\Sigma\Delta$), the timing model, the design-of-experiments, and the acceptance metrics used to extract design rules.

2.1 Quantization at the ADC Stage

The ADC converts the sensed output to a digital word. With finite resolution, the least-significant bit (LSB) introduces a voltage step

$$\Delta V_{\text{ADC}} = \frac{V_{\text{FS}}}{2^{N_{\text{ADC}}}}, \quad (1)$$

where V_{FS} is the ADC full-scale and N_{ADC} is the bit depth. In regulation, bias is typically bounded within about ± 1 LSB [5]. In contemporary designs, meeting ~ 10 mV accuracy at a low-voltage output can require roughly 10–12 bits [2]. If resolution is too coarse, the output dithers around the set point and small errors must accumulate before the controller reacts, slowing small-signal correction.

Low ADC resolution also interacts with the DPWM. If the smallest change the DPWM can produce at the output exceeds ΔV_{ADC} , the loop may never find a zero-error state and instead settle into an LCO. These discrete oscillations inject tones into the spectrum and make EMI harder to predict [3]. Pushing resolution higher at tens of MHz is challenging: high-bit, high-rate sampling increases power, latency, and complexity, motivating careful allocation of bits across the loop rather than simply maximizing ADC resolution.

2.2 Controller Fixed-Point Quantization

Digital controllers are often implemented in fixed-point for efficiency. Coefficients and internal states are stored with a limited number of integer and fractional bits, which perturbs the intended gains and can slightly shift the loop transfer function. If rounding and saturation are not handled carefully, phase/gain margins suffer. In many practical designs, these effects are smaller than those from ADC and DPWM quantizers; nonetheless, the word length must be large enough that coefficient quantization does not introduce material gain or phase error over the intended bandwidth. More fractional bits improve dynamic range and reduce round-off noise, at the expense of silicon cost. In our framework, controller quantization is included explicitly, and we show later that it is rarely the dominant limiter when ADC and DPWM choices are reasonable.

To quantify the sensitivity of the control loop to arithmetic precision, we performed a simulation sweep of the controller word length (W) from 8 to 24 bits for a 1 MHz buck converter scenario. As shown in Figure 1, reducing W below 14 bits leads to numerical saturation and loss of stability, resulting in excessive output ripple. Above 14 bits, the

quantization noise from the controller becomes negligible compared to the ADC and DPWM quantization. Consequently, a word length of 24 bits (with 16 bits for the fractional part) was selected for all subsequent analyses to ensure that arithmetic precision is not the dominant source of error.

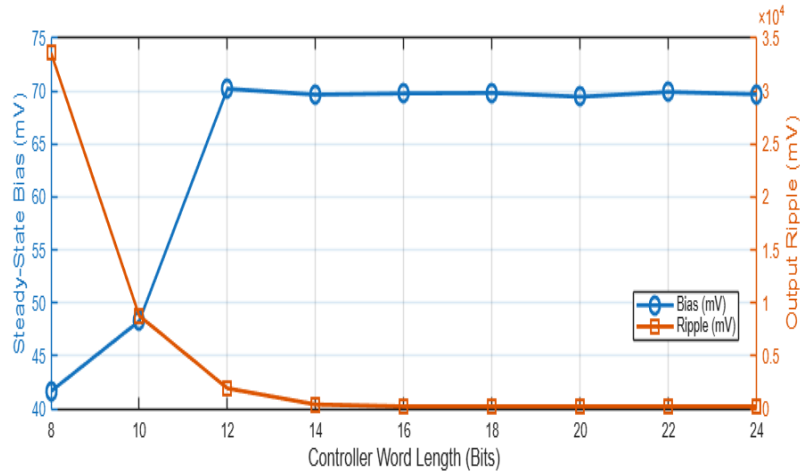


Figure 1. Impact of Controller Fixed-Point Resolution on Performance.

2.3 DPWM Resolution and Dithering

The DPWM converts the controller output into a duty ratio with a finite step of $\Delta D = 1/2^{N_{DPWM}}$ each switching period. Mapped to the output, the smallest duty step produces approximately

$$\Delta V_{DPWM} \approx \left| \frac{\partial V}{\partial D} \right| \frac{1}{2^{N_{DPWM}}}. \quad (2)$$

A widely used rule is therefore to size the DPWM so that $\Delta V_{DPWM} \leq \Delta V_{ADC}$ [1]; if not, one duty step can overshoot an ADC bin and induce LCOs. When a very fine base resolution is impractical, dithering averages between neighboring codes to realize sub-LSB steps on average [2]. Controlled dithering can add roughly one effective bit without a larger DPWM clock, but long patterns push energy to low frequencies (e.g., $f_{sw}/4$ for a 4-cycle pattern), which the output filter attenuates poorly, raising ripple and complicating EMI. First-order $\Sigma\Delta$ modulation is another option: it shapes quantization energy to higher frequencies while preserving average duty, improving effective resolution with a different spectral signature. In all cases, the co-design goal is to obtain enough effective duty granularity without paying an excessive penalty in ripple or clock rate.

2.4 Effects on Performance, Stability, and EMI

Quantization affects operation in three visible ways. First, in steady state, insufficient resolution at the ADC or DPWM forces the output to toggle between discrete levels, lowering accuracy and potentially producing LCOs [1]. Second, in frequency, these oscillations appear as discrete tones that can dominate the ripple spectrum and complicate EMI compliance [3]. Third, in dynamics, small errors may not be corrected until they grow to one LSB, yielding stepped responses and slower settling.

The nonlinearity of quantizers means conventional linear stability margins do not tell the whole story. As shown in prior work, avoiding LCOs requires matching resolution across the loop and managing loop gain [3]. A practical and interpretable condition is to ensure the DPWM step, when mapped through the plant sensitivity $\partial V/\partial D$, is not larger than the ADC LSB; this aligns well with observed no-LCO behaviour in our simulations.

2.5 High-Frequency GaN Converter Trade-offs

At MHz switching, the same quantization issues become more acute. Faster loops shrink the available time for sampling and computation, so latency consumes a larger fraction of T_s . If very fine DPWM steps are demanded at high f_{sw} , the corresponding time

resolution pushes the DPWM clock into the multi-GHz range [1, 4]. That increases digital power and area, and may itself introduce jitter. On the other hand, GaN transitions can be shaped (e.g., resonant or soft-switching) to reduce EMI even as edges get faster [24]. Designers therefore face a coupled trade-off: resolution vs. clocking, latency vs. margin, and filtering vs. spectral placement of quantization artifacts. Our results indicate that modest increases in DPWM resolution (or use of dithering/ $\Sigma\Delta$) together with small delay fractions can preserve stability and millivolt-level regulation at 1–10 MHz, while avoiding the need for extreme clock rates.

2.6 Plant Models and Operating Points

We study three topologies: buck, boost, and inverting buck–boost. Unless stated otherwise, the plant includes capacitor ESR (R_{ESR}), inductor DCR (R_{DCR}), MOSFET on-resistance ($R_{\text{ds(on)}}$), diode forward drop (V_d), and dead-time t_{dead} . Operating points are chosen so that the converter remains in CCM for the cases reported. Switching frequencies are 1, 5, and 10 MHz.

2.7 Digital Control Chain

The loop is fully digital. The ADC samples the sensed output; a fixed-point PI controller with anti-windup updates the duty command; and a DPWM block generates gate pulses. Controller states and coefficients use a word length W and fractional part F . Anti-windup limits the integrator when the duty saturates.

2.8 Quantization Models

The ADC is modeled as a mid-tread quantizer with least-significant bit (LSB)

$$\Delta V_{\text{ADC}} = \frac{V_{\text{FS}}}{2^{N_{\text{ADC}}}}, \quad (3)$$

where V_{FS} is the ADC full-scale and N_{ADC} is the bit depth. The DPWM resolution is $\Delta D = 1/2^{N_{\text{DPWM}}}$ per switching period. The corresponding voltage step is approximated by

$$\Delta V_{\text{DPWM}} \approx \left| \frac{\partial V}{\partial D} \right| \frac{1}{2^{N_{\text{DPWM}}}}. \quad (4)$$

We define

$$\rho \triangleq \frac{\Delta V_{\text{ADC}}}{\Delta V_{\text{DPWM}}} = \frac{V_{\text{FS}}/2^{N_{\text{ADC}}}}{\left| \frac{\partial V}{\partial D} \right| / 2^{N_{\text{DPWM}}}}, \quad (5)$$

and use $\rho \geq 1$ as an interpretable no-LCO guideline. Two DPWM extensions are considered: (i) dither, which averages adjacent codes over a short pattern (e.g., 4 cycles), and (ii) first-order $\Sigma\Delta$, which shapes quantization energy to higher frequencies while preserving average duty.

2.9 Timing and Latency

Sampling and computation delays are modelled explicitly as fractions of T_s : an ADC aperture/sample delay and a digital compute/pipeline delay. Total delay is swept in the 0.03–0.06 T_s range to reflect MHz control pipelines. Dead-time reduces the effective duty by t_{dead}/T_s .

Physically, increasing the loop delay reduces the phase margin, making the converter more susceptible to oscillations and instability, especially at high switching frequencies where the period T_s is very short.

2.10 Design-of-Experiments

The selected switching frequencies (1, 5, and 10 MHz) span the transition from conventional silicon-based designs to modern high-speed GaN applications, allowing us to observe how quantization constraints tighten as the time budget shrinks. For each topology and $f_{sw} \in \{1, 5, 10\}$ MHz we sweep $N_{ADC} \in [N_{min}, N_{max}]$ and $N_{DPWM} \in [M_{min}, M_{max}]$ on a compact grid, with and without dither/ $\Sigma\Delta$. The simulation step is $T_s/200$ to $T_s/500$ and each run spans 2000–3000 periods. A short auto-tune pass picks PI gains that remove DC bias and maintain margin under the chosen delays.

2.11 Metrics and Acceptance Criteria

We record: (i) steady-state bias $|\bar{V} - V_{ref}|$, (ii) output ripple (pk-pk), (iii) limit-cycle occurrence (LCO) via a spectral test that flags dominant tones in $0.02\text{--}0.5 f_{sw}$, (iv) an estimate of $|\partial V/\partial D|$ from small duty perturbations, and (v) the ratio ρ . A configuration is accepted if it satisfies: no LCO, ripple ≤ 10 or 20 mV (as specified), $|\text{bias}| \leq 10$ mV, and $\rho \geq 1$. Heat maps over (N_{ADC}, N_{DPWM}) and a consolidated design-rules table (minimal bit pairs meeting the targets) are reported. In practice, designers can read the maps by selecting ADC/DPWM bit pairs that both satisfy the ripple target and keep $\rho \geq 1$, since points with $\rho < 1$ almost always fall into the LCO-dominated regions.

2.12 Validation Panels

Four checks are used to support validity: (1) analytic vs. simulated $\partial V/\partial D$ over duty slices; (2) ρ -versus-LCO boundary slices at fixed N_{ADC} ; (3) sensitivity to R_{ESR} , L , C , ADC noise, and sampling jitter; and (4) a fixed-point ablation (varying controller fractional bits). These show that the $\rho \approx 1$ boundary aligns with LCO onset, that design rules are robust to moderate parameter variation, and that controller fixed-point is not the dominant limiter.

3. Results and Discussion

We report ripple and limit-cycle behaviour over the (N_{ADC}, N_{DPWM}) grid for three converter topologies (buck, boost, inverting buck-boost) and multiple switching frequencies. Unless stated, plots show V_{out} ripple (pk-pk). When present, a black contour denotes $\rho = 1$; regions to the right/up of this contour tend to be no-LCO and low-ripple.

3.1. Across-Topology Baselines at 1, 5, and 10 MHz

Figure 2 collects the baseline (non-dithered, non- $\Sigma\Delta$) ripple maps for the three topologies at 1, 5, and 10 MHz. As f_{sw} increases, the feasible region shifts toward higher DPWM bits due to tighter timing and larger effective duty sensitivity. At a fixed frequency, boost and buck-boost require finer DPWM than buck for the same ripple target, tracking the larger $|\partial V/\partial D|$. These trends confirm that moving toward multi-MHz operation significantly increases design complexity and hardware demands, because acceptable ripple limits can only be met with higher DPWM resolution and tighter timing control.

3.2. Effective-Resolution Gains from Dither and $\Sigma\Delta$ at 1 MHz

At 1 MHz, both dither and first-order $\Sigma\Delta$ expand the feasible region by roughly one to two effective DPWM bits relative to the baseline; $\Sigma\Delta$ tends to push quantization energy upward in frequency, which can aid EMI if the output filter prioritizes low-frequency attenuation. Figure 3 compares these two techniques across the three topologies at 1 MHz. These benefits, however, rely on an output filter with sufficient high-frequency attenuation; inadequate filter design can significantly reduce the effective advantage of dither or Sigma-Delta modulation.

3.3. Condensed Design Rules

Table 2. lists the minimal (N_{ADC}, N_{DPWM}) pairs that satisfy the acceptance criteria (no LCO, $|\text{bias}| \leq 10$ mV, $\rho \geq 1$) for ripple targets of ≤ 10 and ≤ 20 mV. Baseline entries

are reported at 1/5/10 MHz; dither and $\Sigma\Delta$ entries are reported at 1 MHz. A “–” indicates the criteria were not simultaneously achieved on the scanned grid.

3.4. Interpretation

Three patterns recur across all datasets: (i) the $\rho \approx 1$ boundary aligns with the onset of LCO and delineates low-ripple regions; (ii) boost and buck–boost require higher DPWM resolution than buck at a given ripple target; and (iii) increasing f_{sw} or effective delay shifts the feasible region toward higher (N_{ADC}, N_{DPWM}) . At 1 MHz, modest dither or first-order $\Sigma\Delta$ typically recovers 1–2 effective bits without extreme DPWM clock rates.

3.5. Limitations

This study focuses on establishing the theoretical bounds of quantization in ideal switching conditions. While the simulation model incorporates key non-ideal ties such as delays, R_{on} , and dead-time, it does not account for second-order hardware effects like switching jitter noise or variable EMI filter impedance. However, the derived design rules are intentionally conservative (requiring $\rho \geq 1$). These rules provide a ‘safe operating area’ for designers; if a configuration is stable in this rigorous simulation, it is highly likely to be stable in hardware, though the exact ripple magnitude may vary. Future work will focus on hardware-in-the-loop validation to calibrate these boundaries against experimental GaN prototypes.

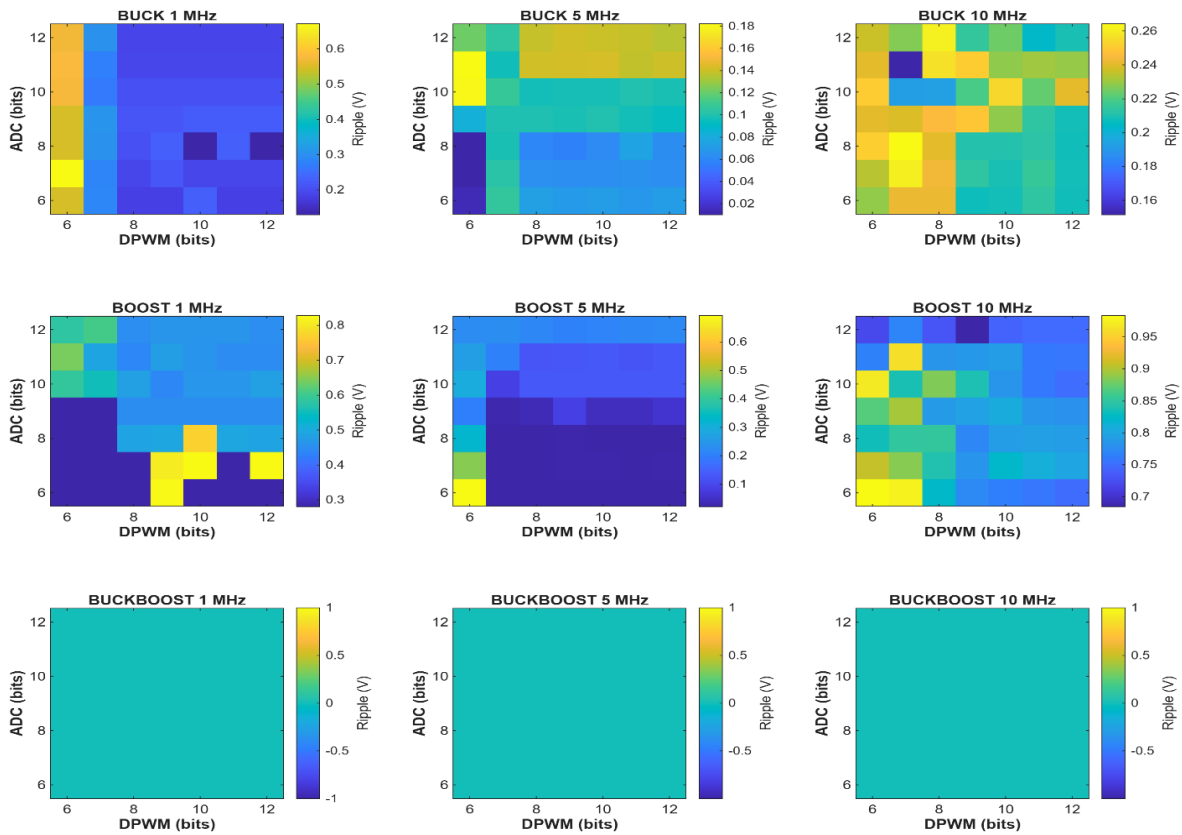


Figure 2. Baseline output voltage ripple maps over (N_{ADC}, N_{DPWM}) at 1, 5, and 10 MHz. Rows represent buck (top), boost (middle), and inverting buck–boost (bottom) topologies. Dark blue regions correspond to stable, low-ripple operation (no limit cycles), while yellow/green regions indicate high ripple or limit-cycle oscillations due to coarse quantization.

Table 2. Minimal $(N_{\text{ADC}}, N_{\text{DPWM}})$ pairs meeting no-LCO, $|\text{bias}| \leq 10 \text{ mV}$, and $\rho \geq 1$ at two ripple targets. Entries show ADC/DPWM bits; “–” indicates not achieved on the scanned grid.

Topology	Mode	f_{sw} (MHz)	$\leq 20 \text{ mV}$	$\leq 10 \text{ mV}$
buck	baseline	1	8/9	–
buck	baseline	5	10/11	–
buck	baseline	10	–	–
buck	dither	1	8/8	11/8
buck	$\Sigma\Delta$	1	8/8	11/8
boost	baseline	1	10/12	–
boost	baseline	5	–	–
boost	baseline	10	–	–
boost	dither	1	9/11	10/11
boost	$\Sigma\Delta$	1	9/11	10/11
Buck-boost	baseline	1	–	–
Buck-boost	baseline	5	–	–
Buck-boost	baseline	10	–	–
Buck-boost	dither	1	–	–
Buck-boost	$\Sigma\Delta$	1	–	–

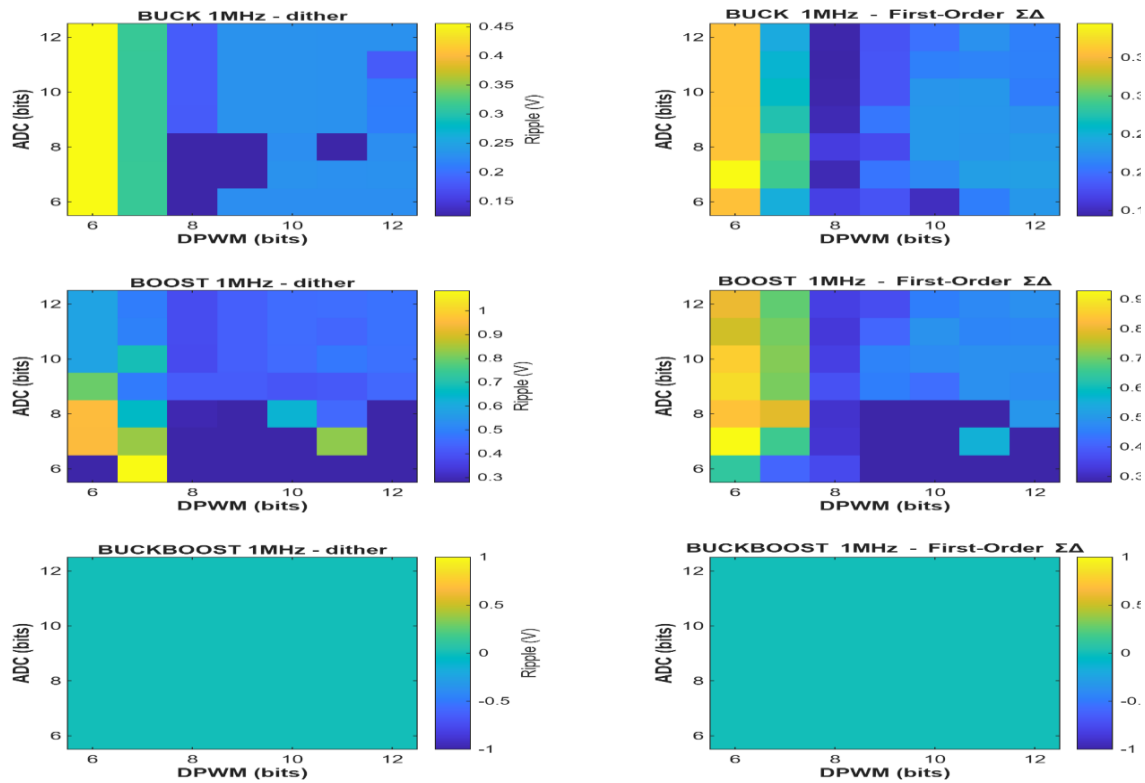


Figure 3. Comparison of dither (left column) and first-order $\Sigma\Delta$ (right column) modulation at 1 MHz for buck (top), boost (middle), and inverting buck–boost (bottom). Both techniques significantly expand the low-ripple (dark blue) region compared to the baseline, allowing for reduced bit depths while maintaining stability.

4. Conclusion

This work studied end-to-end quantization co-design for digitally controlled MHz-range GaN converters, covering the ADC, fixed-point controller, and DPWM. Using a uniform simulation pipeline, we swept (N_{ADC}, N_{DPWM}) across buck, boost, and inverting buck-boost topologies at 1, 5, and 10 MHz. Three consistent findings emerge: first, the $\rho \approx 1$ boundary tracks the onset of limit-cycle oscillations (LCOs); second, boost and buck-boost topologies require higher DPWM resolution than buck due to larger $|\partial V / \partial D|$; and third, increasing f_{sw} shifts the feasible region toward higher bit depths. At 1 MHz, modest dithering or first-order $\Sigma\Delta$ recovers about 1–2 effective bits, relaxing clocking demands. For practitioners, we recommend identifying the smallest bit-pair from the generated ripple maps that satisfies $\rho \geq 1$, then enabling dither/ $\Sigma\Delta$ if the region is tight. While this study is based on conservative, idealized simulations, the derived rules provide a safe starting point for hardware prototyping, with future work planned to validate these findings against parasitic and jitter measurements in GaN experimental setups.

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