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Triple-Level Single-Ended Main Inductor Converter (SeMLC) with regard to Wind-Solar Hybrid Energies

Ariep Jaenul [1, *] and Ban Najm Abdullah Altameemi [2,]

[1] Department of Electrical Engineering, Faculty of Engineering and Computer Science, Jakarta Global University, Depok, Indonesia; ariep@jgu.ac.id
[2] Politehnica University of Bucharest, Bucharest, Romania; ban.altameemi11@gmail.com

Abstract: An output from a DC-to-DC converter that can be more or less than its input is called a Single-Ended Main Inductor Converter (SeMLC). Nevertheless, there is more switching stress in this dual-level SEMIC, which raises switching losses. This rise in switching loss causes the power converter's efficiency to drop. This research suggests a Triple stage SeMIC with lower switching losses to get over this drawback. Using a lower rated switch, Triple level SEMIC increases power efficiency. There is a description of a control method that balances the voltage of the capacitor to avoid damaging the power switch. The suggested converter also lessens the ripple in inductor current in the output inductor. Triple level SeMIC uses a hybrid wind-solar energy system as a source. The benefits of the suggested converter are emphasized by discussing the simulation results of both dual- and Triple-level SeMIC.

Keywords: Hybrid Energy; Solar; Wind Power; Single-Ended Main Inductor Converter (SeMLC)

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1. Introduction

One kind of DC/DC converter that can provide an outcome that is greater or lower than the input amount is the Single-Ended Main Inductor Converter (SeMLC). To separate the input from the output, it makes use of a series capacitor. SeMIC converters' little effort current undulation and energy up/down abilities have made them useful in a variety of industries. The voltage pressure athwart the switches in a dual-level SeMIC converter is equal to the sum of the input voltage (Vi) and output voltage (Vo). Thus, the voltage is under more stress every time the input voltage rises. The overall efficiency of the power converter is reduced as a result of this maximum pressure increasing switching fatalities athwart the switches [1-3].

Triple level SeMIC converters have been designed to address these switching drawbacks. Two parallel capacitors and two series switches are used in these inverters. We can get the total dc link voltage with the aid of these series capacitors [4, 5]. Recently, an isolated Triple-level SeMIC converter was created; nevertheless, the setup costs rise since two transformers are needed [6]. Just half of the total input and output voltage is exerted on the switches in Triple level converters. The operational point of the converter can be ascertained with the use of a PWM SeMIC that has both linked and independent inductors functioning continuously [5].

Because solar energy is pure and endless in nature, it is a sort of renewable energy that is becoming more and more popular. The two most popular ones in use are Free-standing and Network Linked [7]. For energy storage, a battery charger is necessary for a PV solo system. A SeMIC converter may be employed to determine this [8]. Another way to set up a PV generation system is to use a hybrid Triple-level dc-dc converter [5, 9]. Because of its low current input fluctuation and low output voltage fluctuation among

these dc-dc converters, SeMIC has been used for photovoltaic requests [10]. Moreover, the Maximum Power Point Tracking (MPPT) efficiency of SeMIC converters is extremely high. In PV uses, MPPT is utilized to harvest the maximum power that is available at that particular moment [11]. Connecting the PV system to the grid is the difficult part. The system can be connected to the grid using solid state inverters [12]. Two loops make up a three phase, single stage grid-connected photovoltaic system. These are the outer MPPT loop and the PWM loop, which are used to modulate output current [5, 13]. Due to its simplicity of execution, the Perturb and Observe (P&O) method is the most often used algorithm [14]. With the help of this algorithm, which distinguishes between the effects of the tracker's perturbation and the irradiation change, tracking can be optimized in accordance with the irradiation change [15].

The Danish model, which consists of a three-bladed rotor circuitously connected to an power-driven producer by a tackle container, is used by most wind turbines today [11, 16-18].

An effective combination PV and wind structure is far more effective than a single source. Most hybrid systems use batteries to supply electricity during periods when neither the PV system nor the wind are producing energy [11, 12, 19]. There is a block schematic in Figure 1. The suggested system uses Triple level SeMIC converters for transferring the solar arrays and WECS's maximum power.

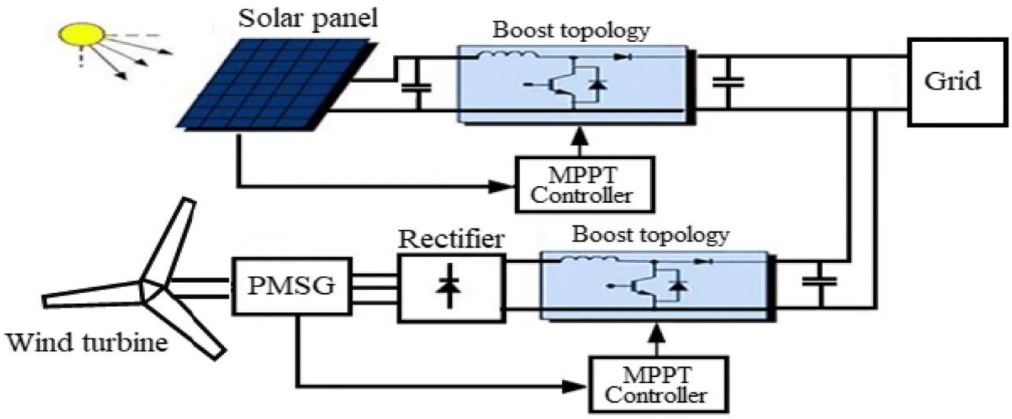


Figure 1: Planned system's block diagram

2. Materials and Methods

2.1 Configuring the Converter

The circuit diagram for the suggested Triple-level SeMIC is displayed in Figure 2(a). It is made up of two switches, Q1 and Q2, two capacitors, C1 and C2, an output inductor, Lo, two diodes, D1 and D2, an input filter capacitor, Cf, an input inductor, and two output capacitors, Co1 and Co2. The insulated-gate bipolar transistors (IGBTs) are designated Q1 and Q2. The midpoint of the output capacitors is linked to the midpoint of the switches that are connected in series. The voltages across Q1 and Q2 are denoted as VQ1 and VQ2, respectively. The voltages across D1 and D2, respectively, are VD1 and VD2. The currents of Li and Lo are, respectively, iLi and iLo. The output voltage Vo is divided into two equal voltages, Vo1 and Vo2, using Co1 and Co2 as a capacitive voltage divider (Vo1 = Vo2 = Vo/2).

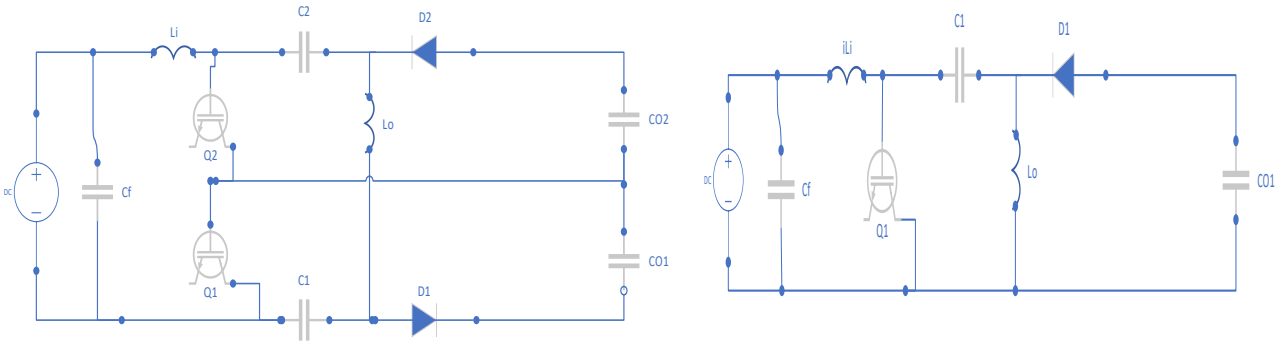


Figure 2 Circuit diagram (**a**) Triple-level (**b**) Dual-level

2.2 Operating Techniques

DQ1 is the pulse width, or duty ratio, of Q1.DQ2 is the pulse width, or duty ratio, of Q2. P1 and P2 pulses are phase-shifted 180 degrees apart.

State 1: When D >0.5, this mode is active. In this mode, D1 and D2 are open and Switches Q1 and Q2 are closed. Energy from the input voltage Vi is stored in the input inductor Li. At a Eq. (1), the input current iLi flows. At a Eq. (2), the output inductor current iLo flows.

state 2: In this state Eq. (2), D1 and Q2 are open, while switches Q1 and D2 are closed. Energy from the input voltage Vi is stored in the input inductor Li. At Eq. (3), the input current iLi flows. Capacitors C1 and C2 are charged by the input inductor current. At Eq. (4), the output current iLo charges C1 and Co2.

$$\frac{diLi}{dt} = \frac{Vi}{Vi} \tag{1}$$

$$\frac{diLo}{dt} = \frac{Vi}{Lo} \tag{2}$$

$$\frac{diLi}{dt} = \frac{Vi - Vo}{2Li} \tag{3}$$

$$\frac{diLo}{dt} = \frac{Vi - Vo}{2Lo} \tag{4}$$

state 3: In this state, D2 and Q1 remain open while switches Q2 and D1 are closed. Power from the input voltage Vi is stored in the input inductance Li. At Eq. (3), the input current iLi flows. Both capacitors C2 and Co1 are charged by the input inductance current. The inductor current at the source charges C2 and Co1.The average speed of flow of this current is at Eq. (4).

State 4: When D<0.5, this state is active. In this mode, D1 and D2 are closed, whereas switches Q1 and Q2 are open. Capacitors Co1 and Co2 receive the energy they have stored from the input inductance Li, which discharges C1 and C2. At Eq. (5), the input current iLi streams. At Eq. (6), the output inductor current iLo occurs.

$$\frac{diLi}{dt} = -\frac{Vi}{Li} \tag{5}$$

$$\frac{diLo}{dt} = -\frac{Vi}{Lo} \tag{6}$$

2.3 SeMIC for Double and Triple Levels

Figure 2 (b) displays the circuit diagram for a dual-level SeMIC converter. An input inductor (Li) and an output inductor (Lo) make up this system. Table 1(b) lists the values of its input capacitance (Ci) and output capacitance (Co). MATLAB simulates the dual-

level SeMIC, and figure 2(b) displays the output voltage. Table 1(a) displays the input parameters for the Triple-level SeMIC.

Table 1 (**a**) limitations for Triple level SeMIC

LIMITATION	STANDARDS
Cf	0.99µF
Li	0.99mH
C1and C2	9.98µF
Lo	0.97mH
Co1 and Co2	679µF

Table 1 (**b**) limitations for Dual level SeMIC

LIMITATION	STANDARDS
Cf	0.99µF
Li	0.99mH
C1and C2	9.98µF
Lo	0.97mH
Co1 and Co2	679µF

2.4 Closed Loop Management: Dual and Triple Level SeMIC

Figure 2(b) depicts the closed loop circuit for the dual level SeMIC. The fault has been sent to the PI controller when the production voltage has been related to a constant value. After comparing the PI controller's output to the repeated indication, pulse is generated for the switch.

The output side of a Triple-level SeMIC contains two capacitors, which are C1 and C2. The voltages of these capacitors ought to be matched. This is the balance the following formula: Vc1 = Vc2 = Vi/2. One unbalanced capacitor could have a voltage that is higher than the switches' failure the voltage, which could seriously harm the electrical power switch. In figure 2(a), the closed loop circuit is displayed. Perturb and Observe (P&O) is the MPPT control that the entire system is now using.

3. Results

3.1 Open Loop Performance for SEMIC Levels dual and Triple

Figure 3 (a) displays the voltage across the switch for the dual level SeMIC. A graph is created by connecting voltage and time. Figure 3(b) displays the output voltage for the dual level SeMIC control in an open loop. There is 99.9V input voltage. Figure 4(a) displays the voltage between switches Q1 and Q2 for the Triple levels of SEMIC. There is a set input voltage of 99.9 V. Figure 4(b) displays the output voltage for the Triple level SeMIC control in an open loop.

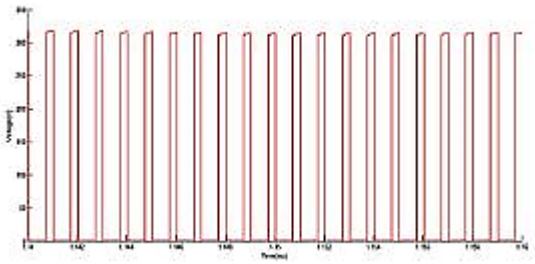
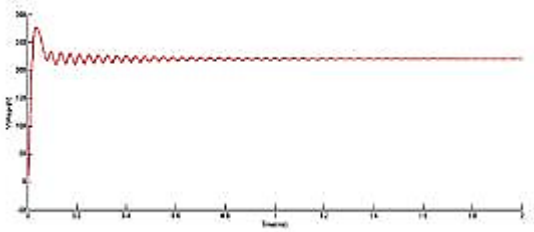


Figure 3 Dual-level SeMIC (**a**) Voltage via the switch



(**b**) Production Voltage in open loop

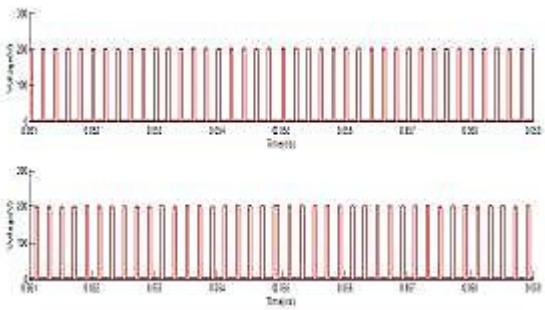
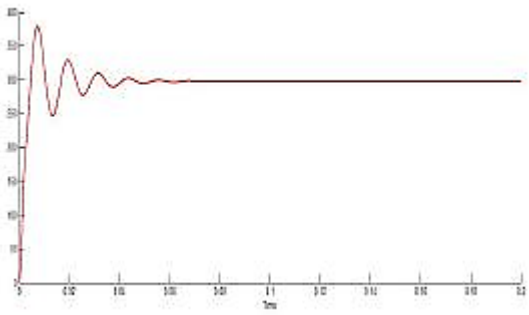


Figure 4 Triple- level SeMIC (**a**) Voltage across the switch



(**b**) Production Voltage in open loop

3.2 Closed Loop Performance for SeMIC at Levels Dual and Triple

The PV and wind panels provide the converter's supply. A three-phase rectifier is employed for converting the wind's electricity to DC. 11.9V is the power that comes from the wind and PV. Figure 5(a) depicts the output voltage for the second stage, and Figure 5(b) depicts the third stage.

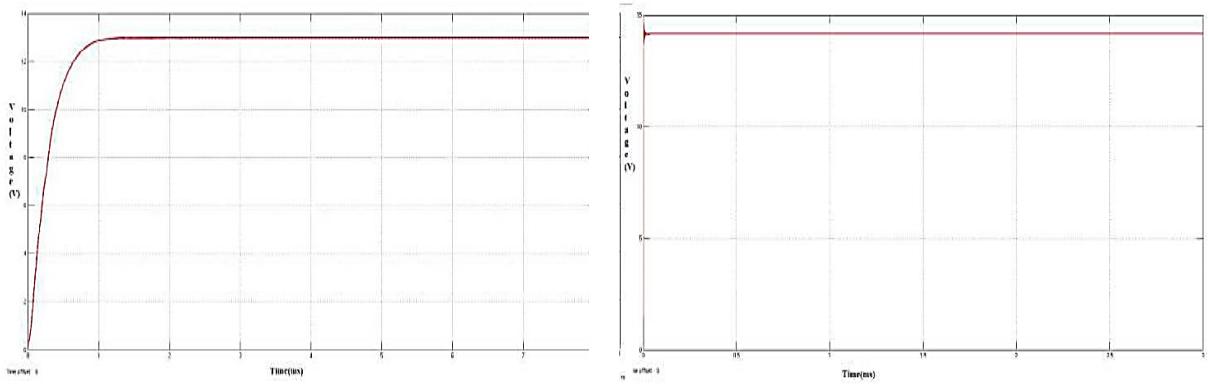


Figure 5 Production voltage (**a**) Dual-level (**b**) Triple-level

Figure 6(a) depicts the ripple in inductor current, and Figure 6(b) shows the Triple levels. For a dual-level SeMIC, the voltage across the switches is 87.9V, the output voltage is 87.9V, and the ripple in the inductor current is 41.9A. For a Triple-level SeMIC, 137.39V is the output voltage, 0.049A is the ripple in the inductor current, and 129.79V is the voltage across the switches.

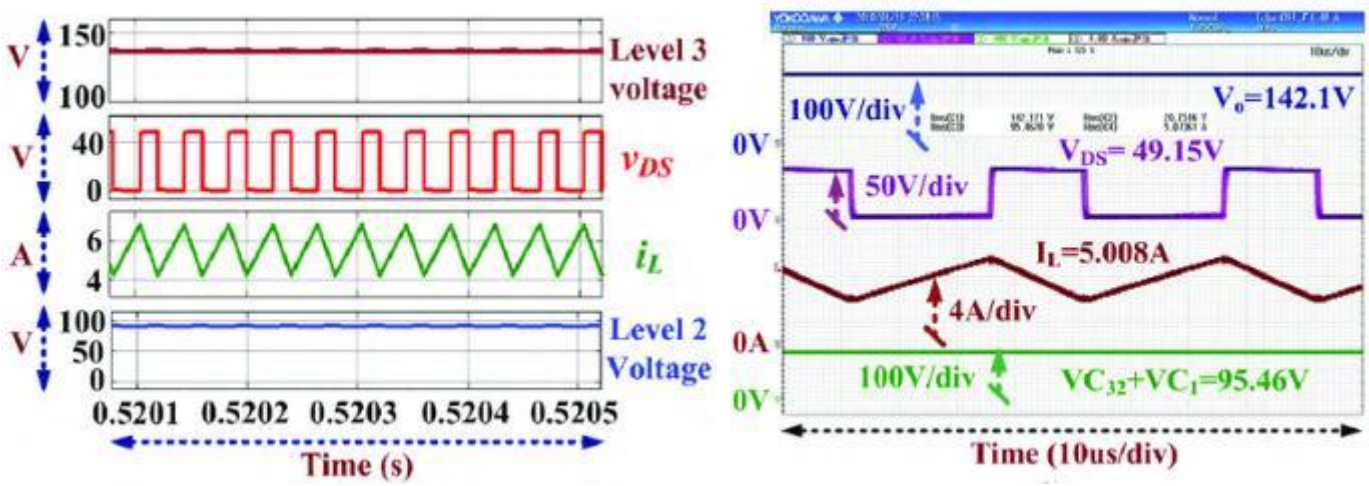


Figure 6 production inductance current (**a**) Dual-level (**b**) Triple-level

3.3 Results get/from Modeling

Table 3 provides information on input, output, and voltage across the switches for both dual- and Triple-level SeMICs. It also shows us just how switching stress is reduced in open-loop, Triple-level SEMICs.

The switching stress against input voltage in an open loop is displayed on the graph in Figure 6. The graph indicates that, in an open loop, the switching stress is higher for levels dual and Triple. Table 4 displays the closed loop results for Triple level SeMIC, while Table 5 displays the findings for dual level SeMIC.

PARAMETERS	VALUE
Input Voltage	11.93 V
Output Voltage	14.19 V
Voltage across the switch	13 V
Theoretical	13.2 V

Table 2 (a) Output of closed loop Triple level

PARAMETERS	VALUE
Input Voltage	11.97 V
Output Voltage	12.94 V
Voltage across the switch	27.96 V
Theoretical	24.98V

(**b**) Output of closed loop dual level

4. Conclusions

In this paper, the suggested Triple level and current dual-level analysis situs in exposed loop have been deliberated. According to these findings, a Triple-level SeMIC converter reduces switching stress on each switch more effectively than a dual-level SeMIC conversion. The closed loop has been intended to balance the voltage of a capacitor. In the suggested closed loop system, a photovoltaic source has been used. The PV source is integrated with an MPPT controller, and a PI controller is used to determine the responsibility rounds for both switches. MATLAB simulation is used to authenticate the converter's operation and efficiency.

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Conflicts of Interest: Declare conflicts of interest or state “The authors declare no conflict of interest.”

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